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EXAMINER	
NGUYEN, TANH Q	

ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/678,554	**Applicant(s)** LIN, PATRICK	
	Examiner Tanh Q. Nguyen	**Art Unit** 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,15-18 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,15-18 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 10, 15-18, 25-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Zaudtke et al. (US 6,654,816).

3. As per claim 1, Zaudtke teaches a peripheral management system, comprising a system chip [210, 228 - FIG. 2], a peripheral I/O control device [234/236, FIG. 2] and a control management device [230, FIG. 2; 801, FIG. 8], said control management device being electrically connected between said system chip and said peripheral I/O device in series [210-230-234/236, 228-230-234/236: FIG.2], and asserting a first processing signal to said peripheral I/O control device in response to a control signal from said system chip in a normally operational state of said peripheral management system, and asserting a second processing signal to said peripheral I/O control device in response to an external control signal in a crash state of said peripheral management system [col. 15, line 37-col. 16, line 50 teaches normal operation between the system chip and the peripheral I/O device, and operation between a handheld device [123, FIG. 1]

and the peripheral I/O device in a crash state of the peripheral management system to obtain information about the crash and/or recover from the crash].

4. As per claims 2, 3, 10, Zaudtke teaches the peripheral management system being part of a computer system [FIG. 2];

the control management device being a baseboard management controller [management processor 801 being used to track the health of the server computer [col. 16, lines 37-39]];

the external control signal is asserted by a remote terminal [the handheld device [123, FIG. 1]] for controlling the operation of the peripheral I/O control device.

5. As per claims 15-18, Zaudtke teaches the control management device asserting a third processing signal in a simulation control state, the third processing signal being transmitted to the system chip in response to another external control signal from the handheld device [col. 16, lines 24-28], the peripheral I/O control device comprising a super I/O control device [234, FIG. 8], and the external control signal is a remote control signal for simulating I/O operation of the super I/O control device [control signal from handheld device emulating a floppy drive through control device [234, FIG. 8]], the third processing signal processing signal being actively generated to be provided for the system chip [drive A is a drive on the south bridge [col. 9, lines 15-26]].

6. As per claims 25-26, the claims generally correspond to claims 1, 10 above, with the peripheral I/O control device comprising a super I/O control device [234, FIG. 8] and the an idle state of the system chip constituting a crash

state of the peripheral management system, and are rejected on the same basis.

7. Claims 1-2, 5, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Omizo (US 6,820,119).

8. As per claim 1, Omizo teaches a peripheral management system [FIG. 2], comprising a system chip [107, FIG. 2], a peripheral I/O control device [111, FIG. 2] and a control management device [116 - FIG. 2], said control management device being electrically connected between said system chip and said peripheral I/O device in series [107-116-111, FIG. 2], and asserting a first processing signal to said peripheral I/O control device in response to a control signal from said system chip in a normally operational state of said peripheral management system [col. 7, lines 39-42; col. 9, lines 10-16; col. 9, lines 25-29: in a normal operational state, the control management device communicates with a management program run by the CPU through the system chip 107 (hence in response to a control signal from the system chip) and sends the information to the peripheral I/O control device (hence asserting a first processing signal to the peripheral I/O control device)], and asserting a second processing signal to said peripheral I/O control device in response to an external control signal in a crash state of said peripheral management system [col. 9, line 59-col. 10, line 9: in a crash state, in response to a write recovery data (hence in response to an external control signal), the control management device writes the recovery data from a terminal 2 through the peripheral I/O device (hence asserting a processing signal to the peripheral I/O control device)].

9. As per claims 2, 5, 10, Omizo teaches the peripheral management system being part of a computer system [FIG. 2];

the system chip being a south bridge chip [107, FIG. 2];

the external control signal is asserted by a remote terminal [terminal 2, FIG. 2].

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zaudtke et al. in view of Galfken et al. (US 5,991,841).

Zaudtke teaches the management processor including an I/O bus [232, FIG. 8] and separate communications to other bus systems [col. 15, lines 50-51], but does not disclose a low pin count (LPC) bus.

Galfken teaches a low pin count bus being used to reduce packaging and system costs, to allow for serial addressing to any address space, to be compatible with existing bus standards, and to allow for simple circuit design [col. 3, lines 6-32].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a low pin count bus in the peripheral management system because the use of such bus would reduce packaging and system costs, allow for serial addressing to any address space, be compatible with existing bus standards, and allow for simple circuit design.

12. Claims 6-8, 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaudtke et al., and alternatively over Zaudtke in view of Mahmoud (US 6,061,745).

13. As per claim 6, Zaudtke teaches the peripheral I/O control device comprising a control management memory [236, FIG. 8] and a super I/O control device [234, FIG. 8], but does not disclose a peripheral I/O control device comprising a system BIOS.

Since it was known in the art at the time the invention was made to place a system BIOS on a memory as a supplement to the system BIOS on the main memory of a computer system to allow for discovery of the source of the problems in the event of a failure that prevents access to the main memory, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a system BIOS on the peripheral I/O control device, as a supplement to the system BIOS on the main memory of the computer system, in order to allow for discovery of the source of the problems and for recovery in the event of a failure.

Furthermore, Mahmoud teaches a system BIOS [24, FIG. 1(a)] being associated with a peripheral I/O control device [22, FIG. 1(a)] to be used for initialization and configuration [col. 1, line 65-col. 2, line 1].

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the peripheral I/O control device to include a system BIOS, as is taught by Mahmoud, in order to facilitate initialization and configuration of the peripheral management system.

14. As per claim 7, since it was known in the art at the time the invention was made to use flash memory because such memory can be rewritten without being removed from the computer system (as is the case with conventional ROM), it would have been obvious to one of ordinary skill in the art at the time the invention was made for the control management memory to be a flash memory and for the system BIOS to be a flash memory because the use of the flash memory allows the control management memory and the BIOS system to be rewritten without being removed.

15. As per claim 8, Zaudtke teaches a super I/O control device for controlling an infrared transceiver [238, FIG. 8], hence a communication port. Since it was known in the art at the time the invention for a single I/O controller to be used to control a plurality of functionalities such as keyboard, mouse, disk drive, and communication port functionalities, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use such an I/O controller, in order to provide keyboard, mouse, and disk drive functionalities - in addition to the communication port functionality.

16. As per claims 23-24, the claims generally include limitations found in claims 1, 10 above with the peripheral I/O control device including a system BIOS (see rejection of claim 6 above) and an idle state of the system BIOS

constituting the crash state of the peripheral management system, and are rejected on the same basis. Zaudtke further teaches modifying set up/status and/or configuration information with the handheld device [col. 16, lines 16-19], hence updating the system BIOS in order to recover from an idle state to a normal state.

17. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omizo in view of Galfken et al. (US 5,991,841).

Omizo teaches a system management bus [103, FIG. 2], but does not disclose a LPC bus.

Galfken teaches a low pin count bus being used to reduce packaging and system costs, to allow for serial addressing to any address space, to be compatible with existing bus standards, and to allow for simple circuit design [col. 3, lines 6-32].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a low pin count bus in the peripheral management system because the use of such bus would reduce packaging and system costs, allow for serial addressing to any address space, be compatible with existing bus standards, and allow for simple circuit design.

18. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omizo.

19. As per claim 25, the claim generally corresponds to claim 1 with the following distinctions: the peripheral I/O device and the crash state of the

peripheral management system of claim 1 being replaced by a super I/O control device and an idle state of the system chip, respectively.

Omizo discloses the peripheral I/O control device being an IrDA interface. Since it was known in the art for an IrDA interface to perform any one or more I/O functions, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the IrDA of Omizo to perform a plurality of I/O functions - hence a super I/O control device.

Omizo discloses an abnormal state where the computer system is stopped by failure [col. 9, lines 30-32; col. 9, lines 59-61]. Since a failure of a computer system is known in the art to encompass an idle state of a system chip - for failure detection and recovery, it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider an idle state of the system chip as a failure - for failure detection and recovery.

20. As per claim 26, Omizo discloses the external control signal being a write recovery data from the IrDA interface of terminal 2, hence a remote super I/O control signal for controlling the I/O operation of the IrDA interface of the computer system [FIG. 2].

Response to Arguments

21. Applicant's arguments filed July 6, 2006 with respect to claims 1-4, 6-8, 10, 15-18, 23-26 have been fully considered but they are not persuasive.

Applicant argued that Zaudtke does not teach the first processing signal or second processing signal being asserted to the peripheral I/O control device, the first processing signal being asserted in response to a control signal from the system chip, and the second processing signal being asserted in response to an external control signal - because Zaudtke teaches the management functions system 230 only responding to a signal from handheld device 123, regardless of the computer system is in a normal or a crash state.

Applicant's arguments are not persuasive because applicant essentially agreed that Zaudtke teaches the management functions system 230 responding to a signal from handheld device 123 in a crash state - hence a second processing signal being asserted to the peripheral I/O control device in response to an external signal in a crash state. Furthermore, since Zaudtke teaches the management functions system being able to communicate with the host operating system and/or the system ROM [col. 15, lines 41-45], Zaudtke essentially teaches the management functions system responding to a control signal coming from the host in a normal state. Since the system chip is located between the host and the management functions system [FIG. 2], the management functions system would respond to a control signal from the system chip and assert a first processing signal to the peripheral I/O control device.

22. Applicant's arguments with respect to claim 5 have been considered but are moot in view of the new ground(s) of rejection. Furthermore, applicant's arguments with respect to claims 1-2, 4-5, 10, 25-26 are also moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 26, 2006

TQN
July 26, 2006